REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 2-3, 5-10, 12-23 and 25-32 are now pending with claims 5, 7, 12, 18, 22-23, 25 and 30 being independent. Claims 2-3, 5-7, 9-10, 12-17, 19-22, 25, 29, and 32 have been amended.

Claims 5-7, 9-10, 12, 19, 22, 25, and 29 have been amended in response to the Examiner's rejections under 35 USC § 112.

Claims 2-3, 13-17, 19-21, and 32 have been amended to correct capitalization errors and other informalities.

Applicant thanks the Examiner for indicating that claims 5-6, 9-10, 12-13, 19-21, 25-29, and 32 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. § 112, second paragraph and to include all of the limitations of the base claim and any intervening claims. Applicant has rewritten claim 5 to incorporate the elements of claims 1 and 4 into claim 5 and put claim 5 into independent form, thus making claim 5 allowable. Applicant has also amended claim 22 to incorporate the elements present in original claims 4 and 5, thus making claim 22 allowable.

Applicant has rewritten claim 12 to incorporate the elements of claim 11 into claim 12 and put claim 12 into independent form, thus making claim 12 allowable.

Applicant has rewritten claim 25 to incorporate the elements of claim 24 into claim 25 and put claim 25 into independent form, thus making claim 25 allowable.

Claims 2-3 and 6; 13-17; and claims 26-29 each depend from one of independent claims 5, 12, and 25, respectively, discussed above. Accordingly, dependent claims 2-3 and 6; 13-17; and 26-29 are allowable for the reasons set forth with respect to their respective independent claims, and for containing allowable subject matter in their own right. Independent consideration and allowance of the dependent claims are requested.

Amended claim 7 describes a method for conversion of direct stream digital (DSD) signals to pulse code modulated (PCM) signals. The method includes receiving a first plurality of bits from the DSD signal and performing a look-up in a table with a first word in the first plurality of bits to generate a result. The method also includes adding the result to generate a

sum and performing another look-up in the table with a second word in the first plurality of bits and adding the result to the sum until a look-up with a last word in the first plurality of bits is performed and the result added to the sum. The sum is output as a first multiple bit PCM value. The method further comprises receiving a second plurality of bits from the DSD signal and converting to a second multiple bit PCM value using the steps described above until all bits in the DSD signal have been converted.

Independent claims 7, 18, 23, and 30 stand rejected under 35 U.S.C. § 103(a) as obvious over Lim et al. (US 2002/0075953) further in view of Le Ngoc et al. (U.S. Patent 5,175,819). Applicant requests reconsideration and withdrawal of this rejection for at least the reason that neither Lim nor Le Ngoc describes or suggests conversion of DSD signals to PCM signals as described in the steps of receiving a first plurality of bits from the DSD signal, outputting the sum as a first multiple bit PCM value, and receiving a second plurality of bits from the DSD signal and converting to a second multiple bit PCM value using the steps described above until all bits in the DSD signal have been converted.

Lim in the Abstract and in Figure 3 describes a finite impulse response filter for outputting filter output data of 8 bits with respect to filter input data of 4 bits that includes four shifting and storing units. The shifting and storing units unify bits of filter input data of 4 bits. Lim also describes a first selection unit for selecting any one of the input data stored in the four shifting and storing units, an address generating unit for generating addresses of lookup tables corresponding to each of a plurality of filter coefficients groups, first to fourth lookup table groups for generating filter outputs of each filter coefficients group. In addition, Lim describes four accumulating units for shifting the filter outputs of the filter coefficient groups in parallel from the first to the fourth lookup table groups, and second selection unit for serially converting the outputs from each of the four accumulators in accordance with filter coefficients groups. Lim does not describe or suggest conversion of DSD signals to PCM signals using a multiplierless finite impulse response filter. Paragraph 3 in Lim describes use of a pulse forming interpolation filter to suppress inter-symbol interference. Paragraph 3 further describes that the output of four channels is multiplied by a gain and added together so that the result undergoes an orthogonal complex quadrature phase shift keying (OCQPSK) modulation. No part of the Lim reference describes or suggests conversion of DSD signals to PCM signals and more particularly

receiving a first plurality of bits from the DSD signal, outputting the sum as a first multiple bit PCM value, and receiving a second plurality of bits from the DSD signal and converting to a second multiple bit PCM value using the steps described above until all bits in the DSD signal have been converted. For at least these reasons, Applicant respectfully submits that claims 7, 18, 23, and 30 are patentable over Lim.

Le Ngoc fails to remedy the failure of Lim to describe or suggest conversion of DSD signals to PCM signals and more particularly receiving a first plurality of bits from the DSD signal, outputting the sum as a first multiple bit PCM value, and receiving a second plurality of bits from the DSD signal and converting to a second multiple bit PCM value using the steps described above until all bits in the DSD signal have been converted. Le Ngoc in the Abstract describes a parallel to serial converter that includes a FIFO buffer for storing words of data. The converter includes a tap-shift register portion and a data-shift-register portion for converting from parallel to serial format words of data stored in the FIFO buffer. The tap-shift register portion controls the conversion process, receives a serial-input-expansion input signal, and develops a serial-output-expansion output signal. No part of the Le Ngoc reference describes or suggests conversion of DSD signals to PCM signals. For at least these reasons, Applicant respectfully submits that claims 7, 18, 23, and 30 are patentable over Le Ngoc.

Claims 8-10; 19-21; and 31-32 depend from independent claims 7, 18, and 30, respectively. Accordingly, Applicant requests reconsideration and withdrawal of the rejections for claims 8-10, 19-21, and 31-32 for at least the reasons discussed above with respect to claims 7, 18, and 30.

In view of these remarks and amendments, Applicant submits that this application is in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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